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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/041,601	01/10/2002	Kiyoshi Nakai	XA-9596	5105

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EXAMINER	
NGUYEN, THINH T	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/041,601	Applicant(s) NAKAI ET AL.	
	Examiner Thinh T Nguyen	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED OFFICE ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed (see MPEP paragraph 606.01).

A title such as-- MEMORY SEMICONDUCTOR DEVICE WITH REDUCED SENSE AMPLIFIER AREA -- is suggested.

2. The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant cooperation is requested in correcting any errors of which the applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102(b/e) that form the basis for the rejections under this section made in this office action.

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 1-8,10,13-14,16, 19-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakano et al. (U.S. Patent 5629887)

REGARDING CLAIM 1

Nakano et al. (the abstract, fig 15,fig 16, column 5 lines 42-51) disclose a semiconductor integrated circuit device comprising: (a) a first memory array area which includes a plurality of first memory cells and first data lines which are formed on a first layer and connected with the first memory cells; (b) a second memory array area which includes a plurality of second memory cells and second data lines which are formed on the first layer and connected with the second memory cells; (c) a sense amplifier area which includes sense amplifiers; (d) a first connecting area located between the first memory array area and the sense amplifier area; and (e) a second connecting area located between the second memory array area and the sense amplifier area, wherein the semiconductor integrated circuit device further includes: (f) first lines which are formed on a second layer different from the first layer and connected with the first data lines in the first connecting area; and (g) second lines which are formed on the second layer and connected with the second data lines in the second connecting area, the sense amplifiers being connected between the first lines and the second lines and adapted to amplify voltage differences between the first lines and the second lines.

REGARDING CLAIM 2

Nakano et al. (the abstract, fig 15,fig 20) disclose a semiconductor integrated circuit device wherein the first memory array area, the first connecting area, the sense amplifier area, the second connecting area, and the second memory array area are located to align in this order in the extending direction of the first and second data lines.

REGARDING CLAIM 3

Nakano et al. (the abstract, fig 20) disclose a semiconductor integrated circuit device wherein the first memory array area, the first connecting area, the sense amplifier area, the second connecting area, and the second memory array area are areas having virtually rectangular shapes, wherein the semiconductor integrated circuit device further includes a switch forming area, which is located between the first memory array area and the first connecting area, wherein the switch forming area includes data transfer lines (IO) and switch circuits having signal transfer paths, which are connected, between the first data lines and the data transfer lines, the data transfer lines being formed on the second layer to extend in a direction, which intersects the first lines.

REGARDING CLAIM 4

Nakano et al. (fig 4) disclose a semiconductor integrated circuit device wherein the first and second lines (fig 4 reference 11,12) are laid out over the sense amplifier area.

REGARDING CLAIM 5

Nakano et al. (fig 2) disclose a semiconductor integrated circuit device wherein wherein at least part of the first and second lines are laid out over the sense amplifier area.

REGARDING CLAIM 6

Nakano et al. (fig 3,fig 4) disclose a semiconductor circuit wherein the second layer is an upper layer relative to the first layer.

REGARDING CLAIM 7

Nakano et al. (fig 15,fig 20) disclose a semiconductor circuit wherein the first and

second lines are formed to extend in the extending direction of the first and second data lines.

REGARDING CLAIM 8,14

Nakano et al disclose (the title) a DRAM or Dynamic Memory semiconductor device and the fact that a DRAM having word lines which intersect the first and second data lines at right angles, with the memory cells being formed at all intersections of the first and second data lines and the word lines and each made up of a data transfer MISFET and a capacitor, with the gate electrode of the MISFET being connected to a word line are inherent characteristics of a Dynamic Random Access Memory.

REGARDING CLAIM 10,16

Nakano et al. (fig 15) disclose a semiconductor integrated circuit device wherein the first and second data lines have virtually equal line spacing.

REGARDING CLAIM 13

Nakano et al. (the abstract, fig 15,fig 16, column 5 lines 42-51) disclose a semiconductor integrated circuit device comprising: (a) first data lines that are formed to extend in a first direction on a first layer and connected with a plurality of first memory cells; (b) second data lines which are formed to extend in the first direction on said first layer and connected with a plurality of second memory cells; (c) first lines which are formed to extend straight in the first direction on a second layer different from said first layer and connected with said first data lines; (d) second lines which are formed to extend straight in the first direction on said second layer and connected with said second data lines; and (e) sense amplifiers, which are connected to said first lines and said second lines and adapted to amplify voltage differences between said first lines and said second lines.

REGARDINMG CLAIM 19

Nakano et al. (the abstract, fig 15,fig 16, column 5 lines 42-51) disclose a semiconductor integrated circuit device comprising: (a) first data lines, which are formed to extend in a first direction on a first layer and connected with a plurality of first memory cells; (b) second data lines which are formed to extend in the first direction on the first layer and connected with a plurality of second memory cells; (c) first lines which are formed to extend straight only in the first direction on a second layer different from the first layer and connected with the first data lines; (d) second lines, which are formed to extend straight only in the first direction on the second layer and connected with the second data lines; and (e) sense amplifiers which are connected to the first lines and the second lines and adapted to amplify voltage differences between the first lines and the second lines, the first and second lines being laid out over the sense amplifiers.

REGARDING CLAIM 20

Nakano et al. (the abstract, fig 20,column 12 lines 25-35) disclose a semiconductor integrated circuit device comprising: (a) first data lines, which are formed to extend in a first direction on a first layer and connected with a plurality of first memory cells; (b) second data lines which are formed to extend in the first direction on the first layer and connected with a plurality of second memory cells; (c) sense amplifiers, which amplify voltage differences between the first data lines and the second data lines; (d) first lines which are formed to extend in the first direction on a second layer, which is an upper layer relative to the first layer, and are connected between the first data lines and the sense amplifiers; (e) second lines which are formed to extend in the first direction on the second layer and connected

between the first data lines and the sense amplifiers; and (f) precharge lines (VBLR) adapted to feed a precharge voltage to the first and second data lines, wherein the precharge lines are formed to extend in a second direction perpendicular to the first direction on the first layer.

REGARDING CLAIM 21,22,23

Nakano et al. disclose all the invention of a Dynamic Random Access memory device except going into detail about the Power, Ground connections of the sense amplifiers. Theses features, however, are inherent to semiconductor memory device with sense amplifier.

REGARDING CLAIM 24,25,26

Nakano et al. disclose all the invention of a Dynamic Random Access memory device except going into detail about the switching areas of the sense amplifiers. Theses features, however, are inherent to semiconductor memory device with sense amplifier as shown in the abstract and fig 7 of Isobe et al. (US patent 6,046,924).

Claim Rejections - 35 USC § 103

5. The following is a quotation of U.S.C. 103(a) which form the basis for all obviousness rejections set forth in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 9,11,12, 15,17 ,18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano et al. (U.S. patent 5,629,887) in view of further remark.

REGARDING CLAIM 9,15

Nakano et al.(the abstract, fig 15,fig 16, column 5 lines 42-51) disclose all the invention except the use of a Levenson's mask to form the data lines. This feature, however is considered obvious since it is old and well known in the art . A person skilled in the art at the time the invention was made would know how to use a phase shifting Levenson's mask to make semiconductor device without any special teachings.

REGARDING CLAIM 11,12,17,18

Nakano et al.(the abstract, fig 15,fig 16, column 5 lines 42-51) disclose all the invention except for the line spacing minimum dimension or the size of the using the 2F and 4F square rules. This feature, however is considered obvious since it is old and well known in the art . A person skilled in the art at the time the invention was made would know how to use the 2F and 4F square rule to make the semiconductor memory device without any special teachings.

7. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and the page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

8. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to be abandoned (see M.P.E.P. 710.02(b)).

9. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d) which papers have been placed of record in the file.

CONCLUSION

10. The prior arts made of record and not relied upon are considered pertinent to applicant disclosure: Tomishima et al.(US patent 5,325,336) disclose a semiconductor device having power line arranged in a meshed shape.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose phone number is (703) 305-0421. The Examiner can normally be reached on Monday to Friday from 8.30 A.M. to 5.00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, David C. Nelms can be reached on (703) 308-4910. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Thinh T. Nguyen TTN

Art Unit 2818

HOAI HO
PRIMARY EXAMINER